URN etd-0407109-183723-1885
Author Jian-Hao Chen
Author's Email Address No Public.
Statistics This thesis had been viewed 41 times. Download 0 times.
Department
Year 2003
Semester 2
Degree Master
Type of Document Master's Thesis
Language zh-TW.Big5 Chinese
Title Design and Application of High-resolution Encoders
Date of Defense 0000-00-00
Page Count 102
Keyword
Encoder
Interpolation
Delta-Sigma ADC
Filter

Abstract
The speed and position controls of a motor control system generally employ a high-resolution encoder, which cost is about half that of a motor rated below 1 hp. In order to reduce cost, the internal circuit of an encoder is explored.

In the thesis, the relationship between sine and cosine functions is considered in interpolation to obtain a four-fold frequency of the original. In addition, the detection of rising and falling edges of channel A and channel B of an encoder is utilized to get the other four times in frequency. The sixteen-fold algorithm is implemented by two ways, hardware circuit and microcontroller-based circuit.

Due to the progress of semiconductor manufacture and the theory of delta-sigma modulation, high-resolution and fast-conversion ADCs are available now. They are useful in the encoder circuit, and their outputs are fed to FPGA/CPLD to finish the sixteen-fold interpolation.

Finally, the high-resolution signal is applied to an integrated rotary encoder (IRE) and a continuous variable transmission (CVT) electrical carrier.
Advisory Committee Ming-Shyan Wang - advisor

Kai-Nan Yang - advisor

Files No Any Full Text File.
Date of Submission 2004-07-13